

Introduction

The FFT4T core implements a 128 point complex FFT and IFFT over multiple data streams in hardware.

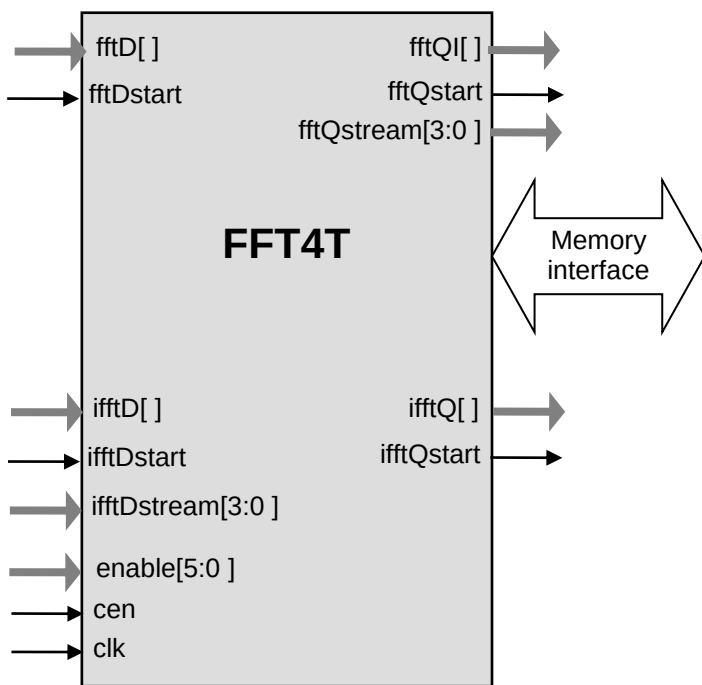
Features

- Supports 128-point complex streaming FFT and IFFT operating simultaneously
- Input and output data are in the natural order
- Multiple streams on input, with optional offset by using a 50% (64 samples) overlap.
- Throughput of 1 sample (In-phase I + quadrature Q) per sample clock for each of the input streams; no-gap processing of the input data
- Input of FFT and output of IFFT are parallel streams (multiple samples, one for each of the streams in parallel)
- Output of FFT and input of IFFT are per-stream, multiple samples in parallel.

Applications

- Signal analysis

Symbol



Pin Description

Name	Type	Description
<i>Common</i>		
clk	Input	Core clock signal (4x sample clock)
cen	Input	Synchronous enable signal. When LOW the core ignores all its inputs and all its outputs must be ignored.
enable[5:0]	Input	RF band enable signals. Each bit controls two streams (path A and path B).
<i>FFT</i>		
fftD []	Input	Input of FFT, Multiple samples in parallel, one for each stream. The samples shall be clocked in on the <i>sample clock</i> .
fftDstart	Input	HIGH pulse clocked on the sample clock indicates the initial 0 sample of the 128-sample frame of fftD
fftQ []	Output	Output of the FFT, multiple samples in parallel. Each stream is output contiguously on sequential <i>sample clocks</i> .
fftQstart	Output	HIGH pulse on sample clock marks the first word of fftQ output (n = 0, samples 0..15) for the stream
fftQstream[3:0]	Output	The value between 0 and 11 indicates the stream number
<i>IFFT</i>		
ifftD []	Input	Input of the IFFT, Multiple samples in parallel. Each stream is clocked in put contiguously on sequential <i>sample clocks</i> .
ifftDstart	Input	HIGH pulse clocked on the <i>sample clock</i> indicates the start of the 128-sample frame (n = 0, samples 0..15) for the stream
ifftDstream[3:0]	Input	The value between 0 and 11 indicates the stream number
ifftQ []	Output	Output of IFFT, 12 samples in parallel, one for each stream. The samples shall be clocked on <i>sample clock</i> .
ifftQstart	Output	HIGH pulse on the <i>sample clock</i> indicates the initial 0 sample of the 128-sample frame of ifftD path A streams

Deliverables

- Synthesizable Verilog RTL source code
- Bit-accurate software model
- Simulation scripts
- Self-checking Test environment
 - Test-bench
 - Test-vectors
 - Expected results



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FFT4T Core

128 Point Multi-stream FFT Core

- Synthesis scripts
- User Manual

Contact Information

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