FFT1024c

Configurable 1024/512 Point FFT Core

Introduction

The FFT1024c core implements 1024 or 512 point FFT in hardware. It can be dynamically configured to process one 1024 or two simultaneous 512 point FFT/IFFT operation.

Features

Supports 512 and 1024-point FFT and IFFT and can switch dynamically

Can process up-to two 512 FFT simultaneously (well suited for MIMO application)

Built-in bit reversal. Outputs in Natural order

Supports reading output data in any order (read address)

Low Latency. Can be customized to improve latency vs. gate count

Throughput of 1 sample per clock

Parameterized bit widths and fixed-point option.

Test bench with fixed-point Matlab model

Available in ASIC and FPGA technologies
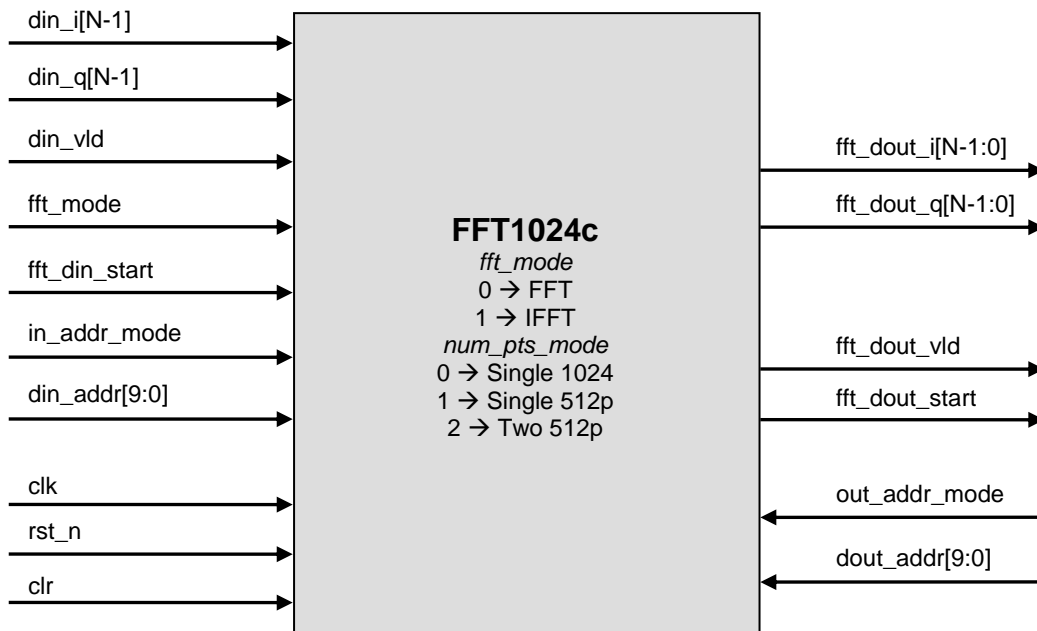
Minimal gate count implementation

Supports flushing and re-starting the FFT operation instantly

Configurable bit width based on SQNR requirement for random inputs or for a specific stimuli pattern.

Customization for OFDM applications

Applications

- WIMAX
- Communication system
- OFDM
- UWB

FFT1024c Block Diagram

Inputs: din_i[N-1], din_q[N-1], din_vld, fft_mode, fft_din_start, in_addr_mode, din_addr[9:0], clk, rst_n, clr

Block: **FFT1024c**
fft_mode
0 → FFT
1 → IFFT
num_pts_mode
0 → Single 1024
1 → Single 512p
2 → Two 512p

Outputs: fft_dout_i[N-1:0], fft_dout_q[N-1:0], fft_dout_vld, fft_dout_start, out_addr_mode, dout_addr[9:0]

Pin Description

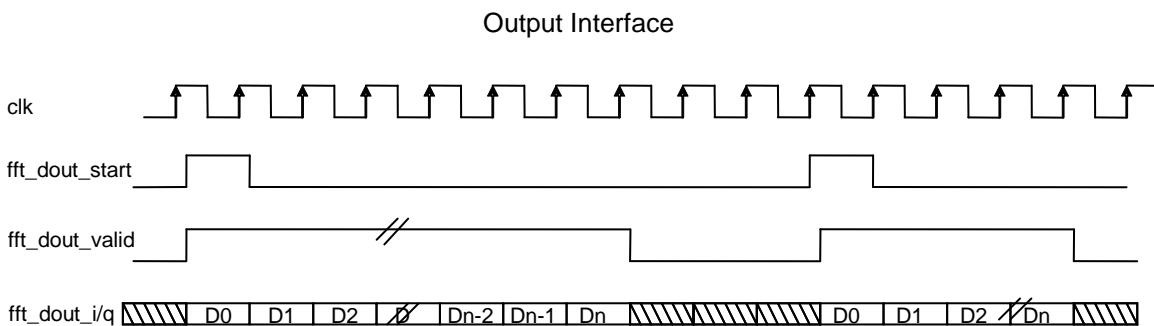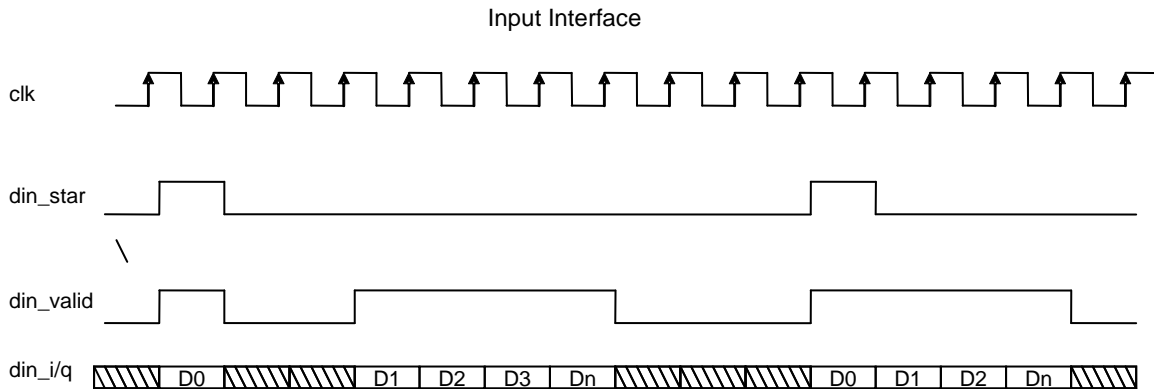| Name	I/O	Width	Description
	1	In	Clock
	1	In	Active low asynchronous reset
CLR	1	In	Active high synchronous reset
FFT_MODE	1	In	0: FFT operation 1: IFFT operation
	2	In	0 → 1024 point FFT/IFFT operation 1 → 1 512 point FFT/IFFT operation 2 → 2 512 point FFT/IFFT operation 3 → Reserved
	N	In	N bit in-phase input data
	N	In	N bit quad-phase input data
	1	In	Input Data Valid
	1	In	Start the FFT computation. This signal should be asserted either on the last input data sample or anytime after sending all input data. Internal FFT engine will start FFT computation when fft_din_start is sampled high on the clock edge. FFT output will be available after fixed latency.
	1	In	Input Address mode. 1'b0 → Use internal addressing to store input data into the internal buffers. 1'b1 → Use external addressing (din_addr) to store input data into the internal buffers.
	10	In	Input address when in_addr_mode is set to 1. In FFT 512 mode, din_addr[9] is ignored.
	1	In	Output Address mode. 1'b0 → Use internal addressing to read the FFT output data from the internal buffers. 1'b1 → Use external addressing (dout_addr) to read the FFT output data from internal buffers.
	10	In	Output address when out_addr_mode is set to 1. In FFT 512 mode, dout_addr[9] is ignored.
FFT_DOUT_I	N	Out	N bit in-phase output data
FFT_DOUT_Q	N	Out	N bit quad-phase output data
FFT_DOUT_VLD	1	Out	Output Data Valid
FFT_DOUT_START	1	Out	Asserted on the first output point of FFT. This signal is asserted after fixed latency from fft_din_start.

Function Description

FFT1024c can process single stream of 1024 pt FFT/IFFT or 2 streams of 512 pt FFT/IFFT simultaneously. FFT1024c supports two different modes of input data/output data streaming.

a. Natural order: In natural order the input buffer addressing is controlled internally. On reset the internal address is set to 0 corresponding to the first fft/ifft input point.
b. In external address mode, (in_addr_mode == 1), the input data is stored inside internal buffer at the location indicated by din_addr.

The FFT or IFFT radix operations start when fft_din_start pulse is sampled high. The FFT data output will be streamed out after fixed latency. The fft_dout_start pulse is asserted on the first output data sample.
Similar to input address mode, output address mode can also be controlled internally or externally by providing dout_addr.

Interface Timing Diagram

Input Interface

clk

din_star

din_valid

din_i/q | D0 | D1 | D2 | D3 | Dn | D0 | D1 | D2 | Dn

Output Interface

clk

fft_dout_start

fft_dout_valid

fft_dout_i/q | D0 | D1 | D2 | Dn-2 | Dn-1 | Dn | D0 | D1 | D2 | Dn

FFT1024c Timing Diagram

Implementation Details

The 10-bit version of the core size starts at less than 50K ASIC gates. The smaller version of the core (-4) exhibit a latency of 1250 clocks, larger (-8) has 420 clock latency. Representative area/resources figures for a 10-bit implementation are shown below. All versions of the core require a 1024 x (2 x bit width) x 2 bits of memory..

Core	Technology	Area / Resources	Latency
FFT1024-10-4	TSMC 90 nm	50K gates	1250
FFT1024-10-8	TSMC 90 nm	100K gates	420
FFT1024-10-8	Xilinx FPGA		420

Deliverables

- Synthesizable Verilog RTL source code
- Fixed-point Octave (Matlab compatible) model.
- Simulation scripts
- Self-checking Test environment
    - Test-bench
    - Test-vectors
    - Expected results
- Synthesis scripts
- User Documentation

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